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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/080,438 | 02/21/2002 | Thomas E. Pearson | 42390P13560 | 8225 |

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| EXAMINER | |
|---|---|
| VIGUSHIN, JOHN B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2827 | |

DATE MAILED: 12/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/080,438 | PEARSON ET AL. |
| | Examiner | Art Unit |
| | John B. Vigushin | 2827 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *5,14,15,23-25,28-32,41-43 and 50-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,15,23-25,54 and 55* is/are allowed.

6)☒ Claim(s) *5,28-32,43,50 and 51* is/are rejected.

7)☒ Claim(s) *41,42,52,53,56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003 and 22 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:



Paper No. 1103

## DETAILED ACTION

### *Claim Objections*

1. Claims 28 and 53 are objected to because of the following informalities:

a) Since amended Claim 28 is a product claim directed to the recessed channels in the interposer, for which the antecedent basis is clearly in amended product Claim 29, and not in method Claim 23, the following further amendment to Claim 28 is recommended to cure the defect:

**In Claim 28, line 1: change "23" to --29--.**

b) Since Claim 53 depends directly from base Claim 5, then the recitation of a "third plurality" and a "fourth plurality" of grooves is indefinite: Where are the *first plurality* and *second plurality* of grooves? Are there *first* and *second* pluralities of grooves contemplated? The following amendments are two distinct ways to cure the defect:

**(i)** One way to make the matter clear is to keep the language of Claim 53 but change the dependency from "claim 5" to --claim 52-- in line 1 of Claim 53;

**OR**

**(ii)** The other way is to keep the dependency of Claim 53 from base Claim 5 but change "third" to --first-- in line 2, and change "fourth" to --second-- in line 4 of Claim 53.

Appropriate correction is required.

## Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

McKenzie, Jr. (US 5,140,745) Alagaratnam et al. (US 6,335,491 B1)

Armezzani et al. (US 6,198,634 B1)

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 29, 28, 30-32 and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by McKenzie, Jr.

As to Claim 29, McKenzie, Jr. discloses, in Fig. 3B: a circuit board substrate member having a first (upper) surface and a second (lower) surface parallel to each other, the substrate further having an edge perpendicular to the first surface and the second surface; a first plurality of conductive contact pads (corresponding and connected to the pin grid array (PGA) 24; Figs. 3B and the male header application of Fig. 3B in Figs. 6 and 7) on the first surface; a second plurality of conductive contact pads on the second surface (as best seen in the male header application of Fig. 3B in

Fig. 5, the second plurality of conductive contact pads corresponding and connected to the surface mount pads 52 of motherboard 54); a plurality of recessed channels 22 in the edge of the substrate member, extending from the first surface to the second surface, each of the recessed channels 22 having a conductive material 34 therein to form a conductive path between one of the first plurality of contact pads and one of the second plurality of contact pads (Figs. 3B and the application of Fig. 3B as the male header in Figs. 5 and 6; col.2: 59-60); a first plurality of grooves 36 defined between each of the conductive structures 34, hence, between the contact pads on the first (upper) surface (Fig. 3B; col.3: 9-12).

As to Claim 28 (considered by the Examiner as depending from Claim 29; see objection set forth above), McKenzie, Jr. further discloses that each of the recessed channels 22 is a portion of a through hole (Figs. 3A and 3B; col.2: 52-63).

As to Claim 30, McKenzie, Jr. further discloses a second plurality of grooves 36 defined between each of the conductive structures 34, hence, between the contact pads on the second (lower) surface (Fig. 3B; col.3: 9-12).

As to Claim 31, McKenzie, Jr. discloses a device to couple an electronic component package 43 (a daughterboard) to circuit board 54, the device comprising a plurality of interposers 42 and 62 (i.e., the application of Fig. 3B as headers 42 and 62; Figs. 4, 5 and 6; col.3: 24-41) coupled to each other (Fig. 5), each being an interposer as recited in Claim 29.

As to Claim 32, McKenzie, Jr. further discloses that interposers 42 and 62 are coupled together to form an array of conductive paths 46 and 64 to couple the electronic component package 43 to circuit board 54 (Figs. 4-6).

As to Claim 51, McKenzie, Jr. further discloses the first plurality of conductive contact pads and the second plurality of conductive contact pads are spaced at an equal pitch (note the pad spacings 44 in Fig. 4 and the pad spacings corresponding to the pin grid array in Fig. 6; see also the disclosure that "contact progression is .050 inches on each side" near the bottom of Fig. 5).

5. Claim 43 is rejected under 35 U.S.C. 102(e) as being anticipated by McKenzie, Jr.

As to Claim 43, Armezzani et al. discloses: a circuit board substrate 1 having a first surface and a second surface parallel to each other (Fig. 1); a first plurality of conductive contact pads 13 and a second plurality of conductive contact pads 13 on the second surface (Fig. 1; col.3: 57-59); a plurality of solid conductive columns 45' through the substrate 1 perpendicular to the first and second surfaces (Fig. 5b), each column 45' in electrical contact with one of the first plurality of contact pads 13; wherein the conductive columns are formed from an alloy of Sn and Pb comprising at least 81% Pb (col.4: 60-61).

### *Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Armezzani et al. in view of Alagaratnam et al.

A) As to Claim 5:

I. Armezzani et al. discloses: a die 61; and an interposer 3 coupled to die 61 and formed from a circuit board substrate (Fig. 1; col.3: 51-59), by which the apparatus can be electrically coupled to a circuit board 69 (Fig. 6; col.6: 42-45), the interposer 3 comprising: a first (upper) surface on which are disposed a plurality of contacts 13 through which the interposer is coupled to chip 61(Figs. 1, 5 and 5b; col.3: 57-59); a second (lower) surface on which are disposed a plurality of contacts 13 through which the interposer is coupled to circuit board 69 (Figs. 1, 5b and 6; col.3: 57-59); a plurality of conductive paths between the first surface and the second surface, each of the conductive paths formed by a solid conductive column 45' through substrate 3 (Figs. 5 and 5b; col.6: 4-7), wherein each of the conductive columns 45' has a composition of Sn and Pb, comprising at least 81% Pb (col.4: 57-61).

II. Armezzani et al. discloses a chip 61 or 59 mounted to the interposer 3, wherein interposer 3 functions as a carrier for directly mounting the chip as well as an interposer between the chip 61 (or 59) and the circuit board 69 (Fig. 6). Armezzani et al. does not teach a package, distinct from the interposer, coupled to die 61 or 59.

III. Alagaratnam et al. discloses, in Fig. 3, a die 206 and a package 204 coupled to the die 206, wherein the package 204 is, in turn mounted to interposer 202 for

connection to circuit board 226, the package 204 functioning as an adapter board for the die, the adapter board package 204 with bumps 212 having a pitch that adapts to, i.e., matches, the bond pad pitch of the circuit board 226, enabling the connection of the die 206, with bumps 210 having a pitch much less than circuit board 226, to the circuit board 226 (the basic "die adapter" concept is readily seen in Fig. 1; col.1: 13-24). The interposer 202 functions to mitigate any thermal expansion mismatch between die package 204 and circuit board 226 (Abstract). In summary, Alagaratnam et al. discloses a die 206, a package 204 coupled to die 206 and an interposer 202 coupled to package 204 and circuit board 226. The Examiner relies on Alagaratnam et al. for the "die adapter" disclosure of a package substrate (i.e., the "die adapter") coupled to the die.

IV. Since both Armezzani et al. and Alagaratnam et al. are both in the electronics packaging art and disclose a structure wherein a semiconductor device is mounted to an interposer which is, in turn mounted to a circuit board, then the use of a package coupled to the die for adapting the bump contact pitch of the die to the bond pad pitch of the interposer would have been readily recognized in the pertinent art of Armezzani et al. in the case of a die in Armezzani et al. having a bump contact pitch smaller than the bond pad pitch of the interposer.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the packaging structure of Armezzani et al. by including a package substrate coupled to the die 59 or 61 and, in turn, to the interposer 3 of Armezzani et al. for the purpose of matching (adapting) the small bump pitch of a

die to the larger bond pad pitch of the interposer, as taught by Alagaratnam et al., in order to use the interposer 3 of Armezzani et al. in conjunction with semiconductor die having smaller pitch than the interposer 3, thus increasing the range of semiconductor types applicable to the packaging structure of Armezzani et al., and thereby enhancing the functionality of the packaging structure of Armezzani et al.

B) As to Claim 50, modified Armezzani et al. discloses that interposer 3 is fixedly coupled to circuit board 69 through Sn/Pb conductive columns 45' through first contact portions 47' (Fig. 6; col.6: 43-46).

***Allowable Subject Matter***

8. Claim set **14**, 15, 54 and 55, and Claims set **23**-25 have been allowed.

9. Claim set *41*, 42, 56, and Claims 52 and 53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim set **14**, 15, 54 and 55, patentability resides in **the combination of**: **1)** *the interposer comprising a plurality of beams coupled to each other,* **2)** *each beam comprising:* ***(i)*** *a circuit board substrate having a first surface and a second surface,* ***(ii)*** *a first plurality of conductive contacts disposed on the first surface to be coupled to the electronic component package* ***and (iii)*** *a second plurality of conductive contacts*

*disposed on the second surface to be coupled to the circuit board*, in further combination with the other limitations of base Claim 14.

As to Claims **23**-25, patentability resides in *the interposer formed from a plurality of beams coupled to each other, **each** of the beams comprising a circuit board substrate having **the claimed first surface***, in combination with the other limitations of base Claim 23.

As to Claims *41*, 42 and 56, patentability resides in *a first plurality of grooves in the first surface between the conductive columns on the first surface*, in combination with the other limitations of the broadest dependent claim, Claim 41.

As to Claim 52, patentability resides in *a first plurality of grooves in the first surface between the conductive columns*, in combination with the other limitations of the claim.

As to Claim 53, patentability resides in *a "third" [sic] (more appropriately, --first--) plurality of grooves in the second surface between the conductive columns*, in combination with the other limitations of the claim (assuming Claim 53 depends from base Claim 5, as indicated in line 1 of the claim; however, if claim 53 should depend from Claim 52, then the reason for allowance of Claims 52-53 is that indicated for Claim 52, above).

11. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

***Response to Arguments***

12. Applicant's arguments with respect to the rejected claims have been considered but are moot in view of the new ground(s) of rejection.

13. The indicated allowability of claims 29-32 and 43 is withdrawn in view of the newly discovered reference(s) to McKenzie, Jr. (US 5,140,745) and Armezzani et al. (US 6,198,634 B1). Rejections based on the newly cited reference(s) are set forth, above. Accordingly, the present Office Action is made NON-FINAL.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Okada et al. (US 6,534,726 B1) discloses, in Figs.1 and 2, a package substrate 11 having first and second surfaces, component 12 (col.7: 9-12) mounted to the first surface, and having recessed channels 14 in the edge of package 11 for connecting package 11 to a motherboard 5 with solder columns 17 (col.7: 35-37; col.7: 65-col.8: 4). Okada et al. does not teach a first plurality of grooves in the first surface between the contact pads of the first surface. Okada et al. does not teach a composition of the solder, hence, is silent as to whether or not the solder columns 17 are a high melting temperature Pb/Sn solder having a Pb content of at least 81%.

Yamasaki et al. (US 6,080,936) discloses a ceramic interposer 1 having plated through-holes that receive high melting temperature, elliptical solder structures 6 (col.20: 24-25) for connecting an IC chip package 20 (col.12: 10-16) to a circuit board

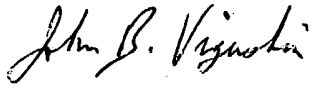
40 (Fig. 6). Yamasaki et al. does not teach that the first surface and second opposite surface have a plurality of contact pads through which the package 20 and circuit board 40 are coupled; i.e., the package 20 and circuit board 40 are electrically coupled to each other directly through the solder structures 6 (Fig. 6).

Goetsch et al. (US 6,098,283) discloses a die 18, a package 16 coupled to die 18, a conductive path formed by a conductive column through the substrate (i.e., the conductive column is the conductive material that fills a via 28), wherein each of the conductive columns comprises solder (col.2: 58-62). Goetsch et al. does not teach a Pb/Sn solder composition of at least 81% Pb (col.2: 58-62).

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205 (Crystal City campus) and 571-272-1936 (Carlyle campus). The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 703-308-1233 (Crystal City campus) and 571-272-1957 (Carlyle campus). The fax phone number for the organization where this application or proceeding is assigned is 703-308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin
Primary Examiner
Art Unit 2827

jbv
December 03, 2003